Electronic Version
Stylesheet Version v1.1.1

[MULTI-CHIP PACKAGE AND MANUFACTURING METHOD THEREOF]

Abstract

A multi-chip package comprising a carrier, at least a package module, an insulation layer and a patterned metallic layer is provided. The package module is mounted onto one of the surfaces of the carrier. The package module has a plurality of stacked chips electrically connected to each other using a flip chip bonding technique. The insulation layer is formed over the surface of the carrier and encloses the package module. The insulation layer has a plurality of via holes linked to the surface of the carrier and the package module. Depth of the via holes in a direction perpendicular to the surface of the carrier is greater than height of the package module in the same direction. The patterned metallic layer is formed over the insulation layer and fills the via holes, serving as interconnecting lines inside the multi-chip package.